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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,784	08/27/2003	Toru Mori	OK1.570	4482
20987	7590	06/06/2005	EXAMINER	
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			TRAN, TAN N	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8m

<b>Office Action Summary</b>	Application No. 10/648,784	Applicant(s) MORI ET AL.	
	Examiner TAN N. TRAN	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on amendment filed on 03/22/05.
- 2a) ☒ This action is FINAL.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6-10 is/are allowed.
- 6) ☒ Claim(s) 1, 3 and 4 is/are rejected.
- 7) ☒ Claim(s) 2 and 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

*Minhloan Tran*  
**Minhloan Tran**  
**Primary Examiner**  
**Art Unit 2826**

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                                                         |                                                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                                                                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                                                    | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>03/22/05; 07/15/04</u> . | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3,4 stand rejected under 35 U.S.C. 102(b) as being anticipated by Numata et al. (6,043,536).

With regard to claim 1, Numata et al. discloses a device comprising an SOI substrate having a SOI layer 7 including a core region (CR) to which a first voltage is applied and an interface region (IR) to which a second voltage is applied; a device separation region 12 for separating the SOI layer 7 into the core region (CR) and the interface region (IR) wherein a thickness of the SOI layer 7 of the core region (CR) is thinner than a thickness of the SOI layer 7 of the interface region (IR), a plurality of first transistors 1B formed in the core region (CR) and in which the SOI layer 7 of the above core region (CR) is a fully depleted Si channel; and a plurality of second transistors 1A formed in the interface region (IR) and in which the SOI layer 7 of the above interface region is a fully depleted Si channel. (Note attachment #1, lines 41,42, column 8; lines 30-33, column 21, fig. 35 of Numata et al.). It is inherent that Numata et al.

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discloses a second driving voltage of an interface region is higher than the first driving voltage of a core region because the structure of Numata et al. is formed the same as that of applicant, thus the structure of Numata et al. has the same functions as the structure of applicant.

With regard to claim 3, Numata et al. discloses a thickness of the SOI layer 7 of the above core region (CR) is 20 nm. (Note attachment #1, lines 40,41, column 21, fig. 35 of Numata et al.).

With regard to claim 4, Numata et al. discloses a thickness of the SOI layer 7 of the interface region (IR) is 1 nm to 0.1 micrometer. (Note previous attachment #1, lines 38,39, column 21, fig. 35 of Numata et al.).

### **Allowable Subject Matter**

2. Claims 2,5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2,5 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as a channel length of the first MOSFET formed in the core region is made shorter than a channel length of the second MOSFET formed in the interface region, the first driving voltage is 1.5v and the second driving voltage is 3.3v as recited in claim 5.

3. Claims 6-10 are allowable over the prior art of record because none of these references disclose or can be combined to yield the claimed invention such as an SOI layer including a high speed computing region to which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied as recited in claim 6.

#### **Response to Arguments**

4. Applicant's arguments filed 3/22/05 have been fully considered but they are not persuasive.

It is argued, at page 10 of the remarks, that "the semiconductor device in Fig.35 of the Numata et al. reference is not described or even remotely suggested as including a core region and an interface region"; "the Numata et al. reference as relied upon by the Examiner does not disclose or even remotely suggest that the device of Fig. 35 includes a core region and an interface region"; "the Numata et al. reference also fails to disclose a plurality of first MOSFETs in a core region having a first driving voltage applied thereto and a plurality of second MOSFETs in an interface region having a second driving voltage applied thereto, wherein the second driving voltage is higher than the first driving voltage"; and "The Numata et al. reference does not specifically disclose core and interface regions, does not disclose respective first and second driving voltages for core and interface regions, and does not disclose a second driving voltage greater than a first driving voltage". However, the previous attachment #1, lines 41,42,

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column 8; lines 30-33, column 21, fig. 35 of Numata et al. do show a device comprising an SOI substrate having a SOI layer 7 including a core region (CR) to which a first voltage is applied and an interface region (IR) to which a second voltage is applied. It is inherent that Numata et al. discloses a second driving voltage of an interface region is higher than the first driving voltage of a core region because the structure of Numata et al. is formed the same as that of applicant, thus the structure of Numata et al. has the same functions as the structure of applicant. Although the applicant uses terms different to those of Numata et al. to label the claimed invention, this does not result in any structural difference between the claimed invention and the prior art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use different terminology to describe the plurality of elements that constitute an integrated circuit as this is just a writing style and the way in which a structural limitation is expressed does not affect the configuration of the described elements. Thus, applicant's claims 1 and 3 do not distinguish over Numata et al. reference.

### **Conclusion**

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

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calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (571) 272-1923. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TT

May 2005